



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/604,821

08/20/2003

Chieng-Chung Chen

11208-US-PA

1820

31561

7590

10/20/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

EXAMINER

HUR, JUNG H

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/604,821

Applicant(s)

CHEN, CHIENG-CHUNG

Examiner

Jung (John) Hur

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 7-10 is/are rejected.
- 7) ☒ Claim(s) 6 and 11 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: search history.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it uses the phrase "are presented" which can be implied. Further, it does not describe the disclosure sufficiently (i.e., it does not describe any key inventive features of the power detector and the power detecting method). It is suggested that the first sentence be deleted, and some key inventive features of the power detector and the power detecting method be added (without the abstract exceeding 150 words in length). Correction is required. See MPEP § 608.01(b).

2. Claim 2 is objected to because of the following informalities: Said claim recites "the second power source" in line 9 of the claim, which appears to be lacking antecedent basis in the claim. For the purpose of further examination, it will be understood as --a second power source--. Appropriate correction is required.

3. Claim 5 is objected to because of the following informalities: Said claim recites "a first output signal" which appears to be referring to that recited in parent claim 2 and should be

Art Unit: 2824

recited as --the first output signal--. It will be understood as such for the purpose of further examination. Appropriate correction is required.

Drawings

4. Figures 6 and 7 should be designated by a legend such as --Prior Art--, because it appears that only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagasawa (U.S. Pat. No. 5,424,994).

Regarding claim 1, Nagasawa, for example in Figs. 4, 5A and 5B, discloses a method of detecting power sources in an integrated circuit (IC), which comprises: receiving a first power

Art Unit: 2824

source (57), and a second power source (58); and discerning (via 50) whether the first received power source is at a pre-determined power level (for example, low or OFF power level for 57), and providing a first output signal (the output of 50) accordingly to indicate a power level of the first power source, wherein when the first output signal indicates that the first power source is at the pre-determined power level (for example, when 57 is in low or OFF power level), a power level of the second power source is detected (via 51 and 53-56; see rows "2" and "3" in Fig. 5B, wherein when the output of 50 is 0, the output of 51 becomes effective), and a second output signal (the output of 51) is provided to indicate a power level of the second power source (58 in Fig. 4), a first state of the second output signal indicates a first power level of the second power source (for example, the 1 state of the output of 51 indicates a full or ON power level for the power source 58; see Fig. 5B), and a second state of the second output signal indicates a second power level of the second power source (for example, the 0 state of the output of 51 indicates low or OFF power level for the power source 58; see Fig. 5B).

Regarding claims 2-5, Nagasawa, for example in Figs. 4, 5A and 5B, discloses a power source detecting circuit for detecting a power source in an integrated circuit (IC), which comprises: a first power source detector (50) for detecting whether the IC operates at a first pre-determined power level (of 57), and providing a first output signal (output of 50); a second power source detector (51) for detecting whether the IC operates at a second pre-determined power level (of 58), and providing a second output signal (output of 51) to indicate a power level of a second power source (58), wherein a first state of the second output signal (the 1 state of the output of 51) allows the IC to operate at a first data power level (that of 58; see also Figs. 5A-

Art Unit: 2824

5B), and a second state of the second output signal (the 0 state of the output of 51) allows the IC to operate at a second data power level (that of battery 16; see also Figs. 5A-5B), wherein the IC is a DRAM (see for example column 2, lines 6-10), wherein the first power source detector receives an external power (from 57) and provides the first output signal to indicate whether the external power allows the IC to function normally (i.e., to indicate the status of 57 which provides power under a normal operating condition).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasawa (U.S. Pat. No. 5,424,994) in view of admitted prior art ("Admission").

Nagasawa discloses a circuit as in claims 2 and 5 above (under 102 rejection), with the exception of: the first output signal changing from a high state to a low state to indicate that the external power source allows the IC to function normally; first, second and third resistors and a MOSFET or bipolar transistor.

Admission, in Fig. 7, discloses a power source detector comprising: first, second and third resistors and a MOSFET transistor, and the output changes from a high state to a low state to indicate that a normal operation (or function) is allowed (see for example instant specification, paragraph 5).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the detector of Admission for the detectors of Nagasawa (for example 50 and 51 in Fig. 4), and therefore, reverse the logic such that, with appropriate modifications, the low state of 50 and 51 would be active, since the detector configuration of Admission was common and well known in the art (for example, as a power-on reset (POR) circuit) as an equivalent, alternative means for detecting a power source. Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to replace the MOSFET transistor with a bipolar transistor, since bipolar transistors were well known in the art as an equivalent, alternative device for controlling and switching purposes.

Allowable Subject Matter

9. Claims 6 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the prior art of record do not disclose or suggest a circuit as recited in claim 6, and particularly, the second power source detector detecting the external data power only when the first output signal indicates that the IC functions normally.

Regarding claim 11, the prior arts of record do not disclose or suggest a circuit as recited in claim 11, and particularly, the specific elements and arrangements of the second power source detector recited in claim 11.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yamaguchi et al. (U.S. Pat. No. 5,874,853) discloses detectors for two power source voltages.

Yasuda et al. (U.S. Pat. No. 5,936,443) discloses various power-on reset (POR) signal generator arrangements for external and internal voltages.

Crotty (U.S. Pat. No. 6,160,431) discloses a power-on reset (POR) circuit for dual supply voltages.

Komatsu (U.S. Pat. No. 6,215,725) discloses an operation mode selection circuit based on a detected power potential.

Yamazaki et al. (U.S. Pat. No. 6,768,354) discloses a power-on detection circuit for a plurality of power supply voltages.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870.

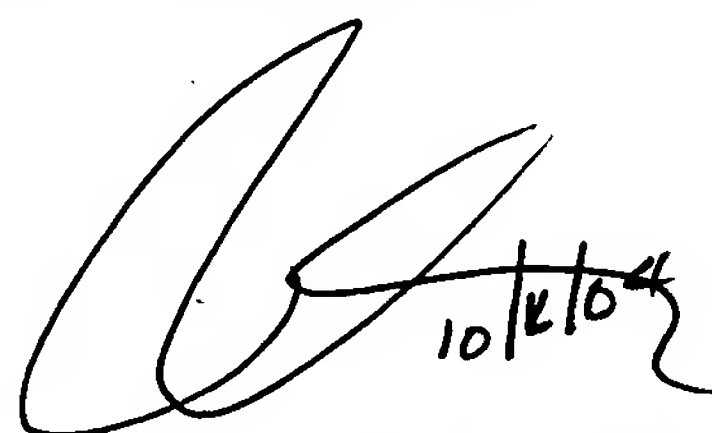
The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh



RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800